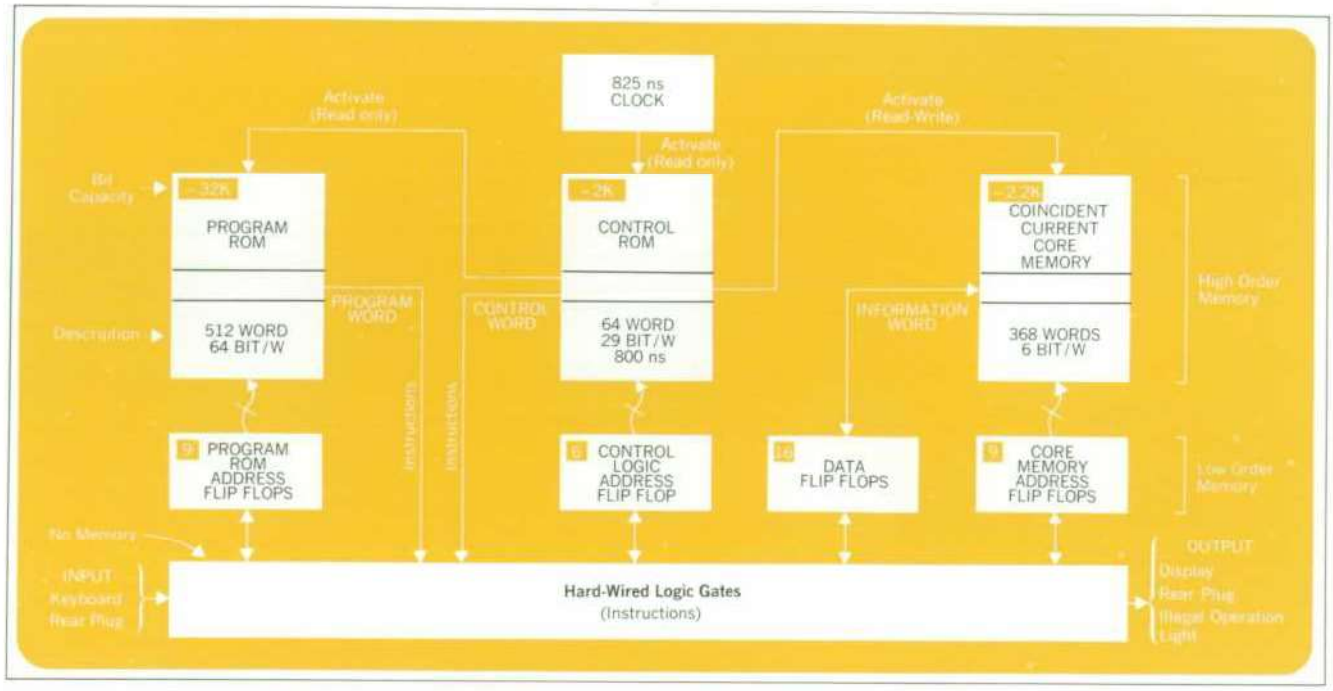

Fig. 1. *Arithmetic processing unit block diagram. This system is a marriage of conventional, reliable diode-resistor logic to a 32,000-bit read-only memory and a coincident current core memory.*

Hardware Design of the Model 9100A Calculator

By Thomas E. Osborne

ALL KEYBOARD FUNCTIONS IN THE MODEL 9100A are implemented by the arithmetic processing unit, Figs. 1 and 2. The arithmetic unit operates in discrete time periods called clock cycles. All operations are synchronized by the clock shown at the top center of Fig. 1.

The clock is connected to the control read only memory (ROM) which coordinates the operation of the program read only memory and the coincident current core read/write memory. The former contains information for implementing all of the keyboard operations while the latter stores user data and user programs.

All internal operations are performed in a digit by digit serial basis using binary coded decimal digits. An addition, for example, requires that the least significant digits of the addend and augend be extracted from core, then added and their sum replaced in core. This process is repeated one BCD digit at a time until the most significant digits have been processed. There is also a substantial amount of 'housekeeping' to be performed such as aligning decimal points, assigning the proper algebraic sign, and floating point normalization. Although the implementation of a keyboard function may involve thousands of clock cycles, the total elapsed time is in the millisecond region because each clock cycle is only 825 ns long.

The program ROM contains 512 64-bit words. When the program ROM is activated, signals (micro-instructions) corresponding to the bit pattern in the word are sent to the hard wired logic gates shown at the bottom of Fig. 1. The logic gates define the changes to occur in the flip flops at the end of a clock cycle. Some of the micro-instructions act upon the data flip flops while others change the address registers associated with the program ROM, control ROM and coincident current core memory. During the next clock cycle the control ROM may ask for a new set of micro-instructions from the program ROM or ask to be read from or written into the coincident current core memory. The control ROM also has

the ability to modify its own address register and to issue micro-instructions to the hard wired logic gates. This flexibility allows the control logic ROM to execute special programs such as the subroutine for unpacking the stored constants required by the keyboard transcendental functions.

Control Logic

The control logic uses a wire braid toroidal core read only memory containing 64 29-bit words. Magnetic logic of this type is extremely reliable and pleasingly compact.

The crystal controlled clock source initiates a current pulse having a trapezoidal waveform which is directed through one of 64 word lines. Bit patterns are generated by passing or threading selected toroids with the word lines. Each toroid that is threaded acts as a transformer to turn on a transistor connected to the output winding of the toroid. The signals from these transistors operate the program ROM, coincident current core, and selected micro-instructions.

Coincident Current Core Read/Write Memory

The 2208 (6 x 16 x 23) bit coincident current memory uses wide temperature range lithium cores. In addition, the X, Y, and inhibit drivers have temperature compensated current drive sources to make the core memory insensitive to temperature and power supply variations.

The arithmetic processing unit includes special circuitry to guarantee that information is not lost from the core memory when power is turned off and on.

Power Supplies

The arithmetic processing unit operates from a single —15 volt supply. Even though the power supply is highly regulated, all circuits are designed to operate over a voltage range of —13.5 to —16.5 volts.

Display

The display is generated on an HP electrostatic cathode ray tube only 11 inches long. The flat rectangular face place measures 3¼" x $4^{13}/_{16}$ inches. The tube was specifically designed to generate a bright image. High contrast is obtained by using a low transmissivity filter in front of the CRT. Ambient light that usually tends to 'wash out' an image is attenuated twice by the filter, while the screen image is only attenuated once.

Fig. 3. *Displayed characters are generated by modulating these figures. The digit 1 is shifted to the center of the pattern.*

All the displayed characters are 'pieces of eight'. Sixteen different symbols are obtained by intensity modulating a figure 8 pattern as shown in Fig. 3. Floating point numbers are partitioned into groups of three digits and the numeral 1 is shifted to improve readability. Zeros to the left of the most significant digit and insignificant zeros to the right of the decimal point are blanked to avoid a confusing display. Fixed point numbers are automatically rounded up according to the decimal wheel setting. A fixed point display will automatically revert to floating point notation if the number is too large to be displayed on the CRT in fixed point.

Multilayer Instruction Logic Board

All of the hard wired logic gates are synthesized on

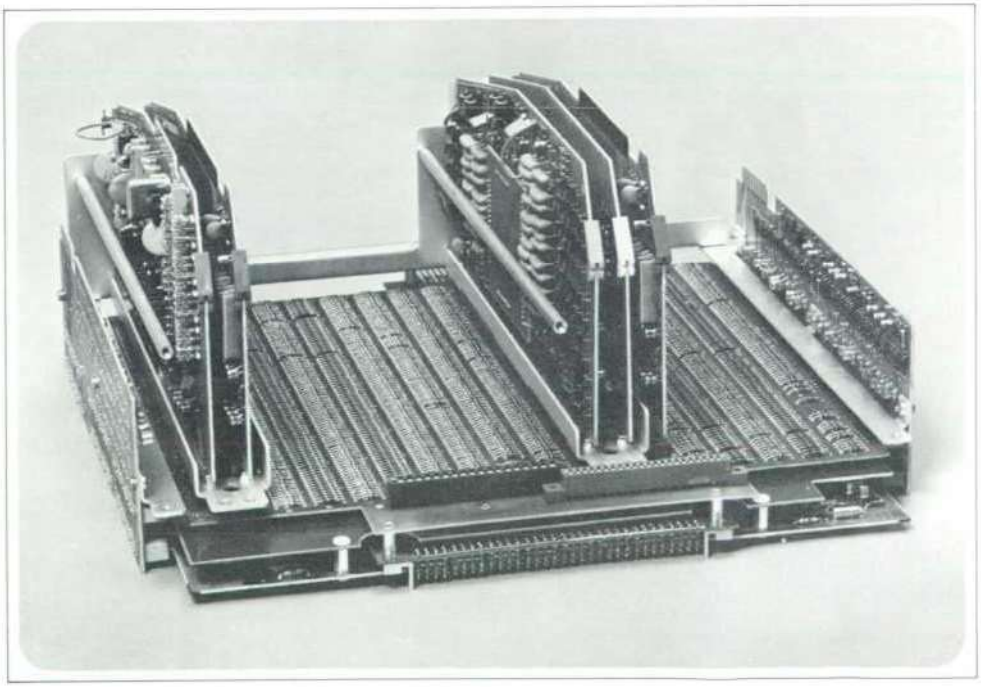

Fig. 2. *Arithmetic unit assembly removed from the calculator.*

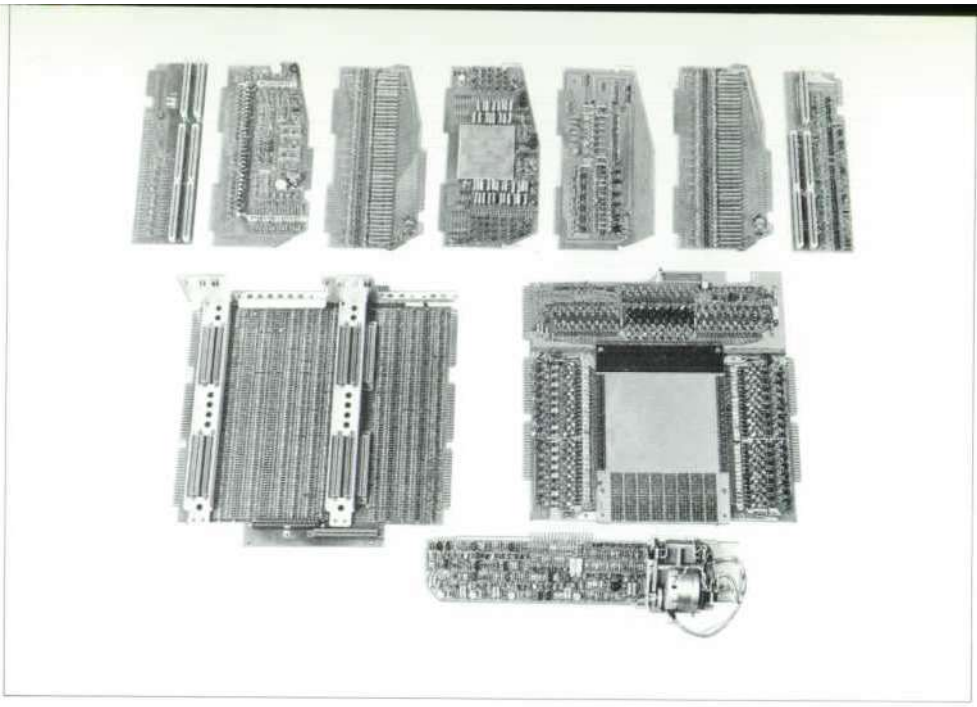

Fig. 4. *Printed circuit boards which make up the arithmetic unit are, left to right at top, side board, control logic, flip-flop, core and drivers, core sense amplifiers and inhibit, flip-flop, and side board. Large board at the lower left is the multilayer instruction board and the program ROM is at the right. The magnetic card reader and its associated circuitry is at the bottom.*

the instruction logic board using time-proven diode-resistor logic. The diodes and resistors are located in separate rows, Fig. 4. All diodes are oriented in the same direction and all resistors are the same value. The maze of interconnections normally associated with the back plane wiring of a computer are located on the six internal layers of the multilayer instruction logic board. Solder bridges and accidental shorts caused by test probes shorting to leads beneath components are all but eliminated by not having interconnections on the two outside surfaces of this multilayer board. The instruction logic board also serves as a motherboard for the control logic board, the two coincident core boards and the two flip flop boards, the magnetic card reader, and the keyboard. It also contains a connector, available at the rear of the calculator, for connecting peripherals.

Flip Flops

The Model 9100A contains 40 identical J-K flip flops, each having a threshold noise immunity of 2.5 volts. Worst case design techniques guarantee that the flip flops will operate at 3 MHz even though 1.2 MHz is the maximum operating rate.

Program Read Only Memory

The 32,768 bit read only program memory consists of 512 64-bit words. These words contain all of the operating subroutines, stored constants, character encoders, and CRT modulating patterns. The 512 words are contained in a 16 layer printed-circuit board having drive and sense lines orthogonally located. A drive line consists of a reference line and a data line. Drive pulses are inductively coupled from both the reference line and data line into the sense lines. Signals from the data line either aid or cancel signals from the reference line producing either a 1 or 0 on the output sense lines. The drive and sense lines are arranged to achieve a bit density in the ROM data board of 1000 bits per square inch.

The program ROM decoder/driver circuits are located directly above the ROM data board. Thirty-two combination sense amplifier, gated-latch circuits are located on each side of the ROM data board. The outputs of these circuits control the hard wired logic gates on the instruction logic board.

Side Boards

The program ROM printed circuit board and the instruction logic board are interconnected by the side boards, where preliminary signal processing occurs.

The Keyboard

The keyboard contains 63 molded plastic keys. Their markings will not wear off because the lettering is imbedded into the key body using a double shot injection molding process. The key and switch assembly was specifically designed to obtain a pleasing feel and the proper amount of tactile and aural feedback. Each key operates a single switch having gold alloy contacts. A contact closure activates a matrix which encodes signals on six data lines and generates an initiating signal. This signal is delayed to avoid the effects of contact bounce. An electrical interlock prevents errors caused by pressing more than one key at a time.

Magnetic Card Reader

Two complete 196 step programs can be recorded on the credit card size magnetic program card. The recording process erases any previous information so that a card may be used over and over again. A program may be protected against accidental erasure by clipping off the corner of the card, Fig. 9, page 8. The missing cor-

Fig. 5. *Internal adjustments of the calculator are easily accessible by removing a few screws and lifting the top.*

ner deactivates the recording circuitry in the magnetic card reader. Program cards are compatible among machines.

Information is recorded in four tracks with a bit density of 200 bits per inch. Each six-bit program step is split into two time-multiplexed, three-bit codes and recorded on three of the four tracks. The fourth track provides the timing strobe.

Information is read from the card and recombined into six bit codes for entry into the core memory. The magnetic card reading circuitry recognizes the 'END' program code as a signal to end the reading process. This feature makes it possible to enter subroutines within the body of a main program or to enter numeric constants via the program card. The END code also sets the program counter to location 0-0, the most probable starting location. The latter feature makes the Model 9100A ideally suited to 'linking' programs that require more than 196 steps.

Packaging and Servicing

The packaging of the Model 9100A began by giving the HP industrial design group a volume estimate of the electronics package, the CRT display size and the number of keys on the keyboard. Several sketches were drawn and the best one was selected. The electronics sections were then specifically designed to fit in this case. Much time and effort were spent on the packaging of the arithmetic processing unit. The photographs, Figs. 2 and 5 attest to the fact that it was time well spent.

The case covers are die cast aluminum which offers durability, effective RFI shielding, excellent heat transfer characteristics, and convenient mechanical mounts. Removing four screws allows the case to be opened and locked into position, Fig. 5. This procedure exposes all important diagnostic test points and adjustments. The keyboard and arithmetic processing unit may be freed by removing four and seven screws respectively.

Any component failures can be isolated by using a diagnostic routine or a special tester. The faulty assembly is then replaced and is sent to a service center for computer assisted diagnosis and repair.

Reliability

Extensive precautions have been taken to insure maximum reliability. Initially, wide electrical operating margins were obtained by using 'worst case' design techniques. In production all transistors are aged at 80% of rated power for 96 hours and tested before being used in the Model 9100A. Subassemblies are computer tested and actual operating margins are monitored to detect trends that could lead to failures. These data are analyzed and corrective action is initiated to reverse the trend. In addition, each calculator is operated in an environmental chamber at 55°C for 5 days prior to shipment to the customer. Precautions such as these allow Hewlett-Packard to offer a one year warranty in a field where 90 days is an accepted standard.

Thomas E. Osborne

Tom Osborne joined HP as a consultant in late 1965 with the responsibility for developing the architecture of the Model 9100A. Previous to joining HP, he had designed data processing equipment, then formed Logic Design Co., where he developed a floating point calculator upon which the Model 9100A is based.

Tom graduated from the University of Wyoming in 1957 with a BSEE, and was named 'Outstanding Electrical Engineer' of his class. He received his MSEE from the University of California at Berkeley.

Tom enjoys flying as a pastime, he is an ardent theater-goer and a connoisseur of fine wines. He is a member of Sigma Tau and Phi Kappa Phi honorary fraternities, and a member of IEEE.